REMARKS

The claims are claims 1, 3 and 4.

Claims 1, 3, and 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Itoh et al (U.S. Patent No. 6.075,941) and Key et al (U.S. Patent No. 6,173,386).

Claim 1 recites subject matter not made obvious by the combination of Itoh et al and Key et al. Claim 1 recites "selectively assigning control of at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program." Regarding claim 1 the OFFICE ACTION states at page 3, lines 9 to 17:

> "Itoh does not expressly disclose selectively assigning control of at least emulation resource of the integrated circuit to one of the serial scan path or the emulation program as claimed. Such feature is however well known in the art. In fact, Key teaches a method and system for debugging a multiprocessor system (col. 4, lines 62-67 and col. 5, Summary of the Invention). The processor debugger selectively assigns control of at least debugging resources of the integrated circuit for emulation into serial scan registers (col. 8, lines 1-12, col. 19, line 39 to col. 20, line 7) in time division multiplexing scheme to determine resource failure in the multiprocessor system and reduce debugging time for such system as taught in Key."

Key et at states at column 8, lines 1 to 12:

> "For IP switching applications, the selector 250 multiplexes fixed-sized units of transient data (e.g., packets) at different rates from all of the cards 240 onto the TDM bus. The multiplexed data is provided to the BQU 210 which extracts a header from the packet prior to loading the packet into the packet memory 220. The BQU then forwards the header to the processing engine 300 over path 290 along with control information specifying the location of the packet in memory 220. Note that in other applications (such as data encryption), the entire packet may be delivered to the processing engine. In the illustrative embodiment, 128 bytes

> of information are forwarded to the engine, of which 64 bytes comprise a network layer (IP) header transmitted over a data portion of path 290 and the remaining 64 bytes comprise control information transferred over a control portion of the path."

The Applicant respectfully submits that this portion of Key et al teaches selection of an input to buffer and queuing control 210 from assorted line cards 240 via multiplexer 250. This is taught in Key et al as a part of the normal operation of router/switch 200. This portion of Key et al fails to mention the claimed "serial scan path." Thus this portion of Key et al cannot make obvious selective assigning of resources to the serial scan path or to the monitor program as recited in claim 1. The Applicant respectfully submits that Key et al at column 19, line 39 to column 20, line 7 teaches a serial scan path according to IEEE standard 1149.1. This portion of Key et al describes resources allocated to this serial scan path. However, this portion of Key et al fails to teach a monitor program. Thus this portion of Key et al cannot make obvious selective assigning of resources to the serial scan path or to the monitor program as recited in claim 1. The OFFICE ACTION states "time division multiplexing scheme to determine resource failure in the multiprocessor system and reduce debugging time for such system as taught in Key" but fails to indicate where this teaching appears in Key et al. Key et al states at column 12, lines 6 to 14:

> "The IHB 700 receives data context from either the data interface of the BQU 210 or from the feedback path 350 and provides the context to each pipeline in succession with feedback data context generally having priority over incoming data context. The data interface preferably includes a path 290 comprising a 128-bit data portion 292 and a control portion 294 for transferring predetermined control signals that manage the flow of data to (and from) the engine."

Thus buffer and queuing unit 210 connects to arrayed processing engine 300 via input header buffer 700. Review of Figure 11 of Key et al shows that this connection causes the inputs from buffering and queuing unit 210 to be entirely separate from the connections of boundary scan test control circuitry 1100. Accordingly, Key et al fails to teach that the multiplexer 250 illustrated in Figure 2 and described at column 8 cooperates with the boundary scan illustrated in Figure 11 and described at columns 19 and 20. Accordingly, claim 1 is not made obvious by the combination of Itoh et al and Key et al.

Claim 3 recites subject matter not made obvious by the combination of Itoh et al and Key et al. Claim 3 recites that selective assigning of emulation resources "assigns said emulation resources to said serial scan path upon a first digital state of said monitor privilege input and assigns said emulation resources to said emulation monitor program upon a second digital state of said monitor privilege input." The OFFICE ACTION states at page 4, lines 1 to 4:

> "As per claim 3, Itoh discloses a monitor program for monitoring priority interrupt, which could include privilege input for monitor program, monitoring privilege interrupt input for the emulation program, and assigning resources for emulation program and path tracing circuit."

The Applicant respectfully submits that Itoh et al does not include any of the terms "monitor program," "monitoring priority interrupt," "privilege input," "monitor program," "monitoring privilege interrupt input," "emulation program" or "path tracing circuit." Without any teaching regarding the claimed monitor privilege input, Itoh et al cannot supplement the teaching of Key et al to make obvious selection according to the monitor privilege input. Accordingly, claim 3 is not made obvious by the combination of Itoh et al and Key et al.

Claim 4 recites subject matter not made obvious by the combination of Itoh et al and Key et al. Claim 4 recites the selectively assigning emulation resources includes "accessing said at least one read write data register." The OFFICE ACTION states at page 4, lines 5 to 9:

> "As per claim 4, Itoh discloses emulation resources and accessing to the emulation resources through read/write data register (Figs. 3-20, col. 8, lines 26-59, cols. 9-13, for example). Key also teaches debugging resource and accessing resources through read and write operations in various data registers (col. 15, line 34 to col. 20, line 50)."

The Applicant agrees that these cited portions of Itoh et al and Key et al disclose emulation resources and accessing such emulation resources by accessing a read write data register. However, the Applicant disputes that these portions of Itoh et al and Key et al teach or make obvious the selective assigning of emulation resources by accessing a read write data register. The Applicant respectfully submits that claim 4 recites a specific function controlled by accessing a register. The cited portions of the references teach a general function of accessing a register without teaching the claimed specific function. Accordingly, claim 4 is not made obvious by the combination of Itoh et al and Key et al.

The Applicant respectfully submits that the rejection of claim 4 as made obvious by the combination of Itoh et al and Key et al fails to comply with the requirements of 37 CFR §1.104(c)(2). The text of 37 CFR §1.104(c)(2) states:

> "(2) In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

The rejection of claim 4 cites 18 figures of Itoh et al in their entirety and 5 columns of text of each of the references Itoh et al and Key et al. The rejection does not refer to particular reference numbers nor any particular structure disclosed. It is difficult for the Applicant to respond to a rejection which cites plural figures and plural columns of the reference as anticipating claimed elements. The Applicant respectfully submits that this rejection clearly fails the requirement that "the particular part relied on must be designated as nearly as practicable." This rejection likewise fails the requirement that "The pertinence of each reference, if not apparent, must be clearly explained." Thus the rejection fails to fulfill the requirements of 37 CFR §1.104(c)(2).

The Applicant respectfully requests a more detailed application of the teachings of the cited references to the features of the claims. The Applicant would greatly appreciate citation of individual reference numbers illustrated in the references for each claimed element. In addition, it would greatly help the Applicant to limit citations to the text of the references to no more than 10 to 15 lines. The Applicant believes that it is the duty of the Examiner under 37 CFR §1.104(c)(2) to provide such detail.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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